

REMARKS

Favorable reconsideration and allowance of the claims of the present application, as amended, is respectfully requested.

At the outset, in the present Office Action, the Examiner indicated that Claims 1-22 remain pending in this case; claims 23-30 being withdrawn. The title of the invention and Claims 1 and 14 reflect changes as per the Examiner's amendment indicated in the Notice of Allowability dated June 29, 2006.

In the present Office Action, the Examiner rejected Claims 1- 22 under 35 U.S.C. 102(a) as being allegedly anticipated by Georgiou et al. reference entitled "A Programmable Scalable Platform for Next Generation Networking" ("Georgiou"). The Examiner indicates in the Office Action that Georgiou teaches the invention as claimed including a microprocessor subsystem for use in an SoC IC comprising a SoC IC communications bus device and standardized components.

Applicants respectfully disagree.

Independent Claims 1 and 14 in their current form, are directed to a self-contained microprocessor subsystem for use in a system-on-chip (SoC) integrated circuit (IC) comprising a processor device, a SoC IC communications bus device and standardized components for enabling communications, said a self-contained microprocessor sub-system. The self-contained microprocessor sub-system is described in Georgiou and is the subject of the current assignee's corresponding U.S. Patent No. 7,072,970. However, respectfully, this paper and patent do not teach the present invention, i.e., its integration in a SoC IC comprising a processor device, a SoC IC communications bus device and standardized components for enabling communications which are described in the present specification with respect to Figures 6 and 7 of the present invention.

The Georgiou reference is directed to the network processor architecture as shown in Fig. 2 which makes up only one component of the SoC IC claimed in the present invention. That is, as claimed in Claims 1 and 14, the present invention is a SoC design that implements a self-contained multiprocessor subsystem core as a self-contained macro. This idea is not disclosed in the above patent or paper. Moreover, the cited reference does not teach or describe the SoC IC having a plurality of processor core assemblies that may communicate with standardized components of an SoC IC via a bridging device as set forth in Claim 1.

In the Office Action, the Examiner cites the Georgiou reference and contends that the teaching is provided at page 2, left column, last line and the next line. Respectfully, this passage is directed to one prior art network processor design having a single embedded PowerPC core and 16 protocol engines. However, this is not a SoC IC design and only comprises one microprocessor (embedded PowerPC core). The improvement is the multiprocessor architecture shown in Fig. 2 of the Georgiou reference. Thus, while the present invention implements the network processor architecture as shown in Fig. 2 of Georgiou, there is no teaching or suggestion of combining and embedding this microprocessor sub-system as a self-contained macro functioning in a device having a processor device, a SoC IC communications bus device and standardized components for enabling communications and protocol conversion at network endpoints to meet performance levels.

In view of the foregoing arguments presented, the Georgiou reference neither teaches nor suggests an SoC system architecture including an independent, self-contained multiprocessor subsystem core as claimed in Claims 1 and 14. As such, the Examiner is respectfully requested to withdraw the rejection of independent Claims 1 and 14 under 35 U.S.C. 102(a) and all claims dependent thereon.

In view of the foregoing, this application is now believed to be in condition for

allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



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